REMARKS

It is submitted, the above made revisions render the present application allowable and, therefore, acceptance/formal entry of the responsive amendment is respectfully requested.

The specification was amended to correct additional informalities noted therein. With these corrective changes, the previously noted objection raised under Item 1a on page 2 of the outstanding Office Action has been rendered moot. A careful reading of the context pertaining to the corrected expressions in paragraph [0061] in the Substitute Specification is consistent with that shown in Fig. 14 of the drawings (which is one phase of the method of manufacture of the semiconductor integrated circuit device) in which the left most portion thereof relates to the memory cell forming region and the silicon oxide film 13 is formed on the surface of the p-type well 5 thereat, consistent with the related description in paragraph [0061] of the Substitute Specification, as now amended.

The claims were amended to further clarify the subject matter intended to be covered including to further highlight various patentable improvements even over that taught by the art documents applied in the outstanding rejection. For example, each of the independent claims 39, 44 and 53 were amended to highlight that the semiconductor substrate can contain both a multiple stage diode formation as well as other active elements such as MISFETs (Metal Insulator Semiconductor Field Effect Transistors) through implementing the diodes such as zener diodes within a semiconductor region or well such as n-type semiconductor region 3 shown in Fig. 4 of the drawings. As can be seen from Fig. 4, n-well (or n-type impurity region) 3 has formed therein both zener diodes D1 and D2. Figs. 20 and 24 give an illustration of

a substrate which contains plural such well regions (or impurity regions) 3, in which the right most region 3 has the diodes such as zener diodes formed therein while other such regions 3 have formed therein other active elements such as MISFETs. For example, in Figs. 20 and 24, the two wells (regions) 3 adjacent to the region 3 containing the zener diodes have MISFETs formed therein, namely, high withstand NMOS and PMOS MISFETs. It is submitted, without such region 3 which acts as an effective isolation region for the multiple stage diodes, it would be, practically, impossible to form other such elements in the substrate.

As is shown in paragraph [0069] and from Fig. 18 of the drawings, other active elements such as MISFETs are formed in different ones of the regions 3 from that having the two series-connected diodes such as the zener diodes formed therein. Such featured aspects are now contained in independent claims 39 and 53 as well as in newly added claim 58 (dependent on independent claim 44). Although independent claim 44 does not specifically set forth a MISFET formed in a separate first impurity region, the claim has been amended to characterize the semiconductor integrated circuit device as one which contains a plurality of first impurity regions (e.g., n-type region 3) in which, also, the plurality of diodes that are connected in series, according to claim 44, are formed in one of the plurality of first impurity regions. Therefore, similarly as that now called for in independent claims 39 and 53, independent claim 44 also sets forth a scheme which effectively isolates (as a result of the presence of the PN junction barriers) the multiple stage diodes from other active elements that may be contained within the substrate of the device.

Additionally, with regard to independent claims 44 and 53, the invention now further calls for the formation of first, second and third wires that are formed from the

same [conductive] layer, consistent with that shown in Figs. 2, 3 and 4 of the drawings and the related discussion directed thereto such as in paragraphs [0047] – [0048] and, further, the discussion in paragraph [0069] and Fig. 18 of the drawings regarding the manufacture of, for example, an LSI which contains EEPROM type memory cells and peripheral circuitry or of a system LSI which also contains bi-polar transistors in the peripheral circuit part of the EEPROM such as shown in Fig. 24 of the drawings, both of which also feature the multiple stage diode such as a zener diode scheme as that of the present invention. It is submitted, the invention as now called for according to claims 39+, 44+ and 53+ is a clear and patentable improvement over that previously known.

As to the outstanding objection of claims 43 and 48, this has now been rendered moot in view of the amendments made thereto. Further, consistent with the amendments made to claims 43 and 48, new claims 56 and 57 were added to cover a complementary conductivity type scheme to that covered by claims 43 and 48.

According to the outstanding Office Action, claims 39-55 were rejected under 35 U.S.C. § 103(a) over the newly formulated combination of references including over Hertrich et al. (USP 4,748,533) in view of Sugawara, et al. (JP 63066974) and Howard, Jr. (USP 3,881,179). It will be shown, hereinbelow, the invention according to that covered by claims 39+, 44+ and 53+ could not have been realized in the manner alleged in the outstanding rejection. Accordingly, this rejection, insofar as presently applicable, is traversed and reconsideration and withdrawal of the same is respectfully requested.

As alluded to hereinabove, the newly presented independent claim groups 39+, 44+ and 53+ are intended to cover a semiconductor IC device scheme calling for two or more series-connected diodes such as zener diodes formed within the same well region (or same impurity region), an example construction of which is given with regard to Figs. 3 and 4 of the drawings, although not limited thereto, which show the formation of a two-stage zener diode for the clamping circuit of Fig. 2 of the drawings. From Fig. 4, it is seen that both diode D1 and diode D2 are implemented within the same n-type region or well 3. This region or well 3 is also shown in the right most portion of the substrate 1 in Figs. 20 and 24, featuring plural ones of such well or impurity regions (e.g. 3).

Insofar as relating to the present claims, diode D2 of the drawings relates to the claimed first diode (first zener diode) while the described diode D1 of Figs. 2 and 4 relate to the claimed second (second zener diode) of the claims. As it relates to independent claim 39+, for example, the p substrate 1 of the drawings relates to the claimed "semiconductor substrate of a second conductivity type," the n-type scattering layer 3 relates to the "first well region," which is doped with phosphorus ions, each of the series-connected zener diodes has its own p wells 5 in Fig. 4 of the drawings, both of which are formed within the n-type layer 3. Also, n^+ region 20 and the underlying p^+ region 6, within each of the p wells 5, relate to the claimed "first semiconductor region" and "second semiconductor region," respectively. With regard to such featured aspects as well as the additional aspects called for in claims 39+ and similarly with regard to other ones of the different claim groupings, paragraphs [0045] – [0048] of the Substitute Specification as well as Figs. 2, 3 and 4 are particularly related thereto. Namely, paragraphs [0045] and [0046] give a

detailed discussion of the example device structure such as it relates to Figs. 3 and 4 of the drawings, in which the conductivity type relationships as well as the size/placement relationships between the p^+ region 6 and that of the n^+ region 20 are given in paragraph [0045] and the relative depth relationships are given in paragraph [0046]. The wire connections as that now called for are discussed in paragraphs [0047] – [0048], etc. It is submitted, the invention called for in claims 39+, 44+ and 53+ was neither taught nor would have been suggested in the manner alleged in the art rejection.

Hertrich, et al. does disclose a series connection of two zener diodes such as zener diodes 3 in Figs. 1 and 2, which are formed in an n^- type region, which is referred to in Hertrich, et al. as a "central base zone of the thyristor." However, Hertrich, et al., it is submitted, did not disclose nor suggest a scheme featuring the formation of wiring layers in connection with the respective diodes in the manner presently called for. Moreover, Hertrich, et al. failed to disclose or suggest that featured aspect of the present invention that would necessitate, in Hertrich, et al., for the respective p wells 14 to be surrounded by a p^- impurity region, synonymous to each p well 5 surrounding each p^+ well 6 in Fig. 4 of the present application. As can be seen from Fig. 2 in Hertrich, et al., the zener diode which consists of n-type semiconductor region 15 and p-type region (p well) 14 is formed in the n^- type semiconductor region 7, which is clearly unlike that presently called for or that shown in Fig. 4 of the present application, which relates to the claimed subject matter of the invention. Unlike a structure according to the present invention, which avoids leakage current problems, Hertrich, et al., it is submitted, neither disclosed nor even hinted at concerns in connection with preventing occurrences of current leakage.

Sugawara, et al. disclosed the formation of a zener diode in a semiconductor substrate (see Fig. 2). According to the scheme shown in Fig. 2, it is apparent that other elements are not to be included in the substrate 1 of Sugawara, et al. There does not appear to be any disclosure or suggestion of the formation of wirings from a single conductive layer to effect the series connection of, for example, two zener diodes nor, for that matter, the implementation of two or more such diodes within the same first well (impurity) region as that presently called for in claims 39+, 44+ and 53+, although such featured aspects are somewhat differently presented with regard to each of these claim groups. With regard to Fig. 2 of Sugawara, et al., n^+ impurity region 10 covers a wider area than p^- region 9, which underlies n^+ region 10. However, Sugawara, et al.'s scheme features a depletion layer 11, which extends deeper than and also surrounds p^- region 9. Moreover, from Figs. 1 and 2 of Sugawara, et al., the connection holes 6 are formed within the area covered by the region 9. It is submitted, therefore, that Sugawara, et al. also failed to teach or even hint at the main aspects of the present invention.

Even if one of ordinary skill in the art would have, arguendo, attempted to consider Hertrich, et al.'s and Sugawara, et al.'s disclosures combinedly, the implementation of two zener diodes in series connection would have been effected as follows:

(a) the two zener diodes would consist of a p^+ semiconductor 11a and an n^+ semiconductor region 10 of Sugawara, et al.;

(b) the two zener diodes would be surrounded around a p^- semiconductor region 2 of Sugawara, et al., and

(c) the p^- semiconductor region 2 would be formed in n^- type semiconductor substrate 1 of Sugawara, et al. and the respective diodes would be isolated by the n^- type semiconductor substrate 1.

It is apparent therefore, such a combination would not have led to a pair of diodes such as a series connected diodes in a manner as that presently set forth where both are formed within a common impurity region or well region but whose structure is effectively isolated as a result of the effective PN junction barriers resulting from the additional impurity or well regions respectively associated with each of the zener diodes.

Howard, et al. disclosed a zener diode structure having an n-type cathode 32, and a p^+ type impurity region 22, which is the anode region, connected with the p-type conductive portion 21. It is noted that the outer peripheral portion of the n-type impurity region 32 is extended deeper than the more central portion of region 32 and that a connection hole C for the cathode is formed on that deeper peripheral region. However, Howard, et al. also did not disclose or suggest implementation of two zener diodes which are connected in series and which are formed in a "first well (impurity) region" formed in a semiconductor substrate.

In fact, the high concentration associated with p^+ anode 22 in Howard, et al. would cause breakdown difficulties if one would have attempted to implement two zener diode scheme. That is, Howard, et al. neither disclosed nor even hinted the key aspects of the invention as that now called for in claim 39+, 44+ and 53+.

Assuming, arguendo, one of ordinary skill would have attempted to combine the teachings of Hertrich, et al., implementation of a multistage diode scheme such as two zener diodes would be effected as follows:

(a) the two zener diodes would consist of a p^+ type semiconductor region 22 and an n^+ type semiconductor region 32 of Howard, Jr., et al.;

(b) the peripheral portion of the n^+ type impurity region 32, in Howard, Jr., et al. would be formed deeper into the substrate than the central portion of the n^+ impurity region 32, of Howard, Jr., et al.;

(c) the two zener diodes would be surrounded around a p^- semiconductor region 2 such as that of Sugawara, et al.; and

(d) the p^- type semiconductor region 2 of Sugawara, et al. is formed in an n^- semiconductor substrate 1 of Sugawara, et al., and each diode is isolated by the n-type semiconductor substrate 1.

In other words, since the zener diode schemes according to Howard, Jr., et al. and Sugawara, et al. are, basically, limited to the formation of single zener diodes and since there does not appear to be any additional teaching therein, or even when combined with Hertrich, et al., regarding the featured wiring connections for effecting a series connection of a pair of zener diodes nor is there any discussion or even a hinting of implementing such a scheme which also enables including other elements in the same substrate while maintaining an effective isolation therebetween, as that which would be effected in connection with the invention in claims 39+, 44+ and 53+, the present invention, as submitted, could not have been rendered obvious even with those combined teachings. As indicated earlier in these remarks, since each zener diode is effectively isolated by the n-type semiconductor 3 that is formed in the substrate 1, the multiple stage zener diode construction can be formed in the substrate 1. Also, with the provision of a plurality of regions such as n-type semiconductor regions 3, in Figs. 4, 20 and 24 of the present application, it allows for

implementation of other elements in the substrate while maintaining an effective operational isolation. Additionally, a wiring scheme such as that presently called for was also not taught even from the combined teachings of Hertrich, et al., Sugawara, et al. and Howard, Jr., et al. Accordingly, the arguments and the rejections notwithstanding, the invention could not have been realizable therefrom.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration and withdrawal of the outstanding objections and rejections, as well as a favorable action on all of the presently pending claims, i.e., claims 39-58, and an early formal notification of allowability of the above-identified application is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned representative at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus,

LLP Deposit Account No. 01-2135 (Docket No. 843.39542X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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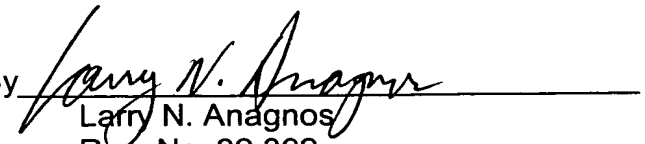
By 
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